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Code No: A5704

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD

M.Tech I Semester Examinations, March/April-2011

ELECTRONIC DESIGN AUTOMATION TOOLS

(VLSI SYSTEM DESIGN)

Time: 3hours **Max. Marks: 60**

Answer any five questions

All questions carry equal marks

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1.a) Explain various constructs for activity flow control with proper examples.
b) Write verilog code for 4 channel multiplexer using 2 different flow controls. [12]

2.a) Differentiate tasks and functions.
b) Write a verilog code for a priority encoder with three state output. [12]

3.a) List - out various cell models available in verilog HDL. Explain about delay cell model.
b) Write a verilog code for D-FF as user defined primitive. [12]

4.a) Define synthesis and performance driven synthesis with respect to verilog HDL.
b) Write a synthesizable verilog code for 4 - bit synchronous counter. [12]

5.a) Explain pulse, piecewise linear, sinusoidal, exponential, Single Frequency Frequency Modulation (SFFM) sources by giving their general syntax and one example.
b) Write a p-spice for a p-MOS inverter. Plot the transient response of the output voltage from 0 to 80 μs insteps of 2 μs. The model parameters of the p-MOS are L=l0, W=20U, VTO = -2, Kp = 4.5E - 4, CBp = -5P_F, CBS = 2p, Rp = 5, Rs = 2, R_B=0, RG =0, RDs = IMEG, CGsp = IPF, CGPP = IPF and CGBp = IPF. [12]

6. Explain the simulation process when a mixed - signal circuit is simulated taking the sample - hold circuit as example. [12]

7.a) Illustrate the basic steps in high speed PCB design.
b) Describe simulation and layout tools in PCB design. [12]

8. Write short notes on any **two**
a) Comparison of VHDL & Verilog.
b) P-Spice model of MOSFET.
c) RAM modeling in verilog. [12]

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